바이오메디컬 시스템반도체 융합설계 인력육성 센터

Chip Design Contest

Face Detection Accelerator Based on Haar Cascade Classifiers

Graduate School of Electronic and Electrical Engineering,
Kyungpook National University

Junghwan Kim, Hayoon Song, Sunghun Jung, and Byungin Moon

Abstract

A face detection algorithm is widely used as a pre-processing system of the face recognition system for extracting only the facial region from the entire image to increase the efficiency of the face recognition operation [1]. In this study, we propose the face detection accelerator based on Haar cascade classifier algorithm to detect only the facial region from an input image acquired by a camera [2]. The proposed face detection accelerator can detect faces of various sizes in the input image by adopting the image pyramid method, and can improve performance by updating internal parameters through I²C-based communication. In addition, the proposed face detection accelerator can be operated with low area and low power through optimization of cascade classifiers. The proposed face detection accelerator operates at a clock frequency of 148.5MHz depending on the operating frequency of the FHD camera module, and outputs face detection results at a rate of 15 frames per second.

Hardware Architecture

Figure 1 shows the hardware architecture of the proposed face detection accelerator. As shown in Figure 1, the proposed face detection accelerator consists of nine modules: 1) Input/Output Interface, 2) Frame Buffer, 3) Scaler, 4) Address Generator, 5) Line Buffer, 6) Integral Image Generator, 7) Cascade Classifier, 8) Merge, and 9) I²C module.

In the Integral Image Generator module, **the word length reduction method [3] was applied to reduce memory usage** by 50% compared with the conventional integral image generation method. To improve the processing speed, the Cascade Classifier module is divided into two-step to **reduce the operation of the first stage** and **reduce unnecessary operations** by adopting the skip scheme in the Cascade Classifier module [2]. In addition, **the performance of the face detection accelerator can be improved** by updating parameters through the I²C module.

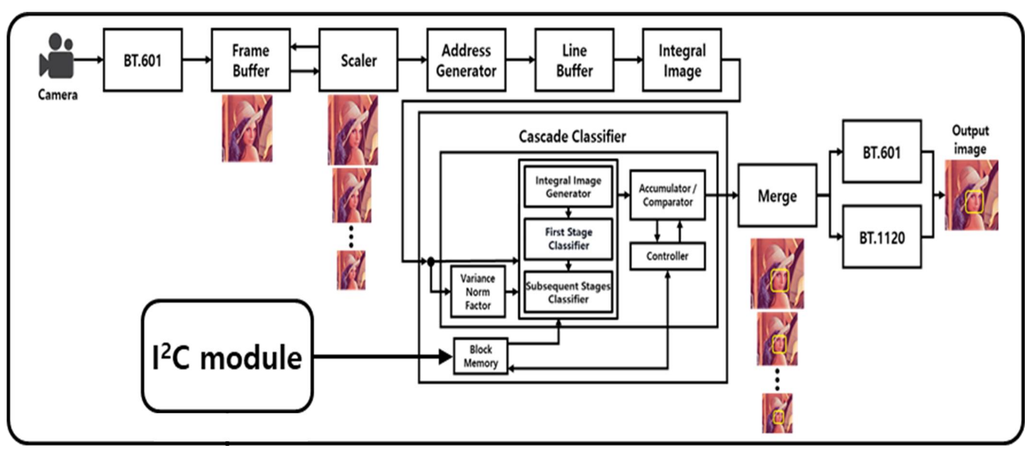


Figure 1. Hardware architecture of the proposed face detection accelerator

Test Environment for FPGA Operation Verification

Figure 2 shows the test environment for verifying operation of the proposed face detection accelerator. The proposed face detection accelerator has been designed using Verilog HDL, and implemented using Xilinx ZC706 FPGA board. The Interface Board receives the FHD video from the Camera and transmits the video to FPGA Board at a clock frequency of 148.5MHz. The FPGA Board stores one image frame that is input from the Interface Board, and outputs the final detection result back to the Interface Board when the face detection is completed. Thereafter, the Interface Board transmits the face detection result to the PC that visualizes and verifies the detection result through a USB interface. The face detection result obtained by implementing the proposed architecture using FPGA is shown in Figure 3.

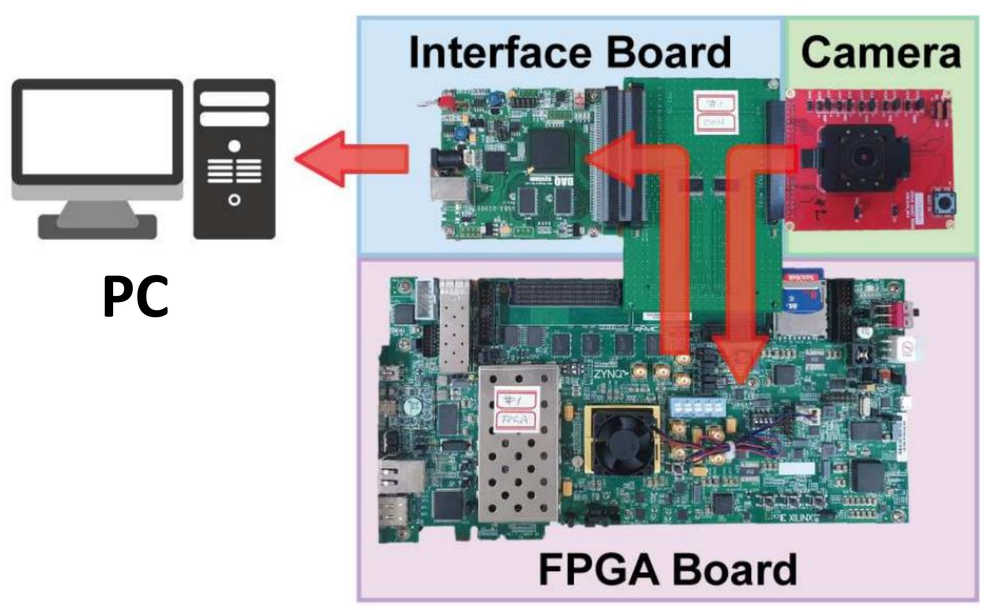
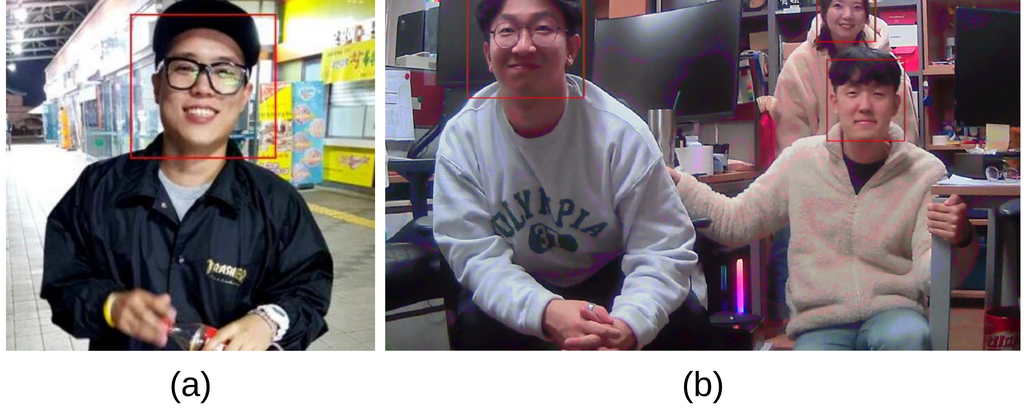


Figure 2. Test environment for verifying operation of the proposed face detection accelerator

Conclusion

In this study, we proposed the face detection accelerator that adopts word length reduction, skip scheme, two-step classifier structure, and I²C-based communication module. The proposed face detection accelerator **can detect faces of various sizes**, and **can improve performance by updating internal parameters**. Moreover, the proposed face detection accelerator **can be operated with low area and low power**. Because of these advantages, the proposed face detection accelerator **can be efficiently used for embedded systems that performs facial image processing**.



(a) (b)

Figure 3. Face detection result: (a) single face detection and (b) multiple faces detection

Reference

[1] P. Viola and M. J. Jones, “Robust real-time face detection,” International journal of computer vision, vol. 57, no. 2, pp. 137-154, 2004.
[2] J. Hyun, J. Kim, C.-H. Choi, and B. Moon, “Hardware Architecture of a Haar Classifier Based Face Detection System Using a Skip Scheme,” in Proc. International Symposium on Circuits and Systems (ISOCC), pp. 1-4, 2021.
[3] J. Kim, J. Hyun, and B. Moon, "Low-cost Hardware Architecture for Integral Image Generation using Word Length Reduction," in Proc. Int. SoC Design Conf. (ISOCC), pp. 119-120, 2020.

Acknowledgement

This research was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (2020M3H2A107804514).

This research was supported by the Multi-Ministry Collaborative R&D program (R&D program for complex cognitive technology) through the National Research Foundation of Korea (NRF) funded by Ministry of Trade, Industry and Energy (NRF-2018M3E3A1057248).

Center for Biomedical System Semiconductor